



BUK9Q12-40H

Logic level N-Channel MOSFET in MLPAK33-WF
(SOT8002-3D)

10 September 2025

Product data sheet

1. General description

Logic level N-Channel MOSFET in a compact MLPAK33-WF (SOT8002-3D) package using Trench 9 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Trench 9 technology - Designed for ruggedness
- Small footprint (3 x 3 mm) for compact design
- Qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automated optical inspection

3. Applications

- Motor drive
- Battery protection
- DC-DC conversion

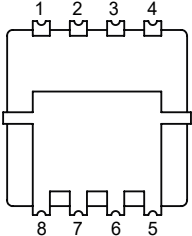
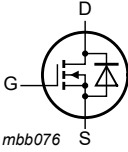
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	41	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	39	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_J = 25\text{ °C}$; Fig. 11	7	10	12	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_J = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	1.4	2.8	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33-WF (SOT8002-3)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Q12-40H	MLPAK33-WF	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Q12-40H	1NG

8. Limiting values

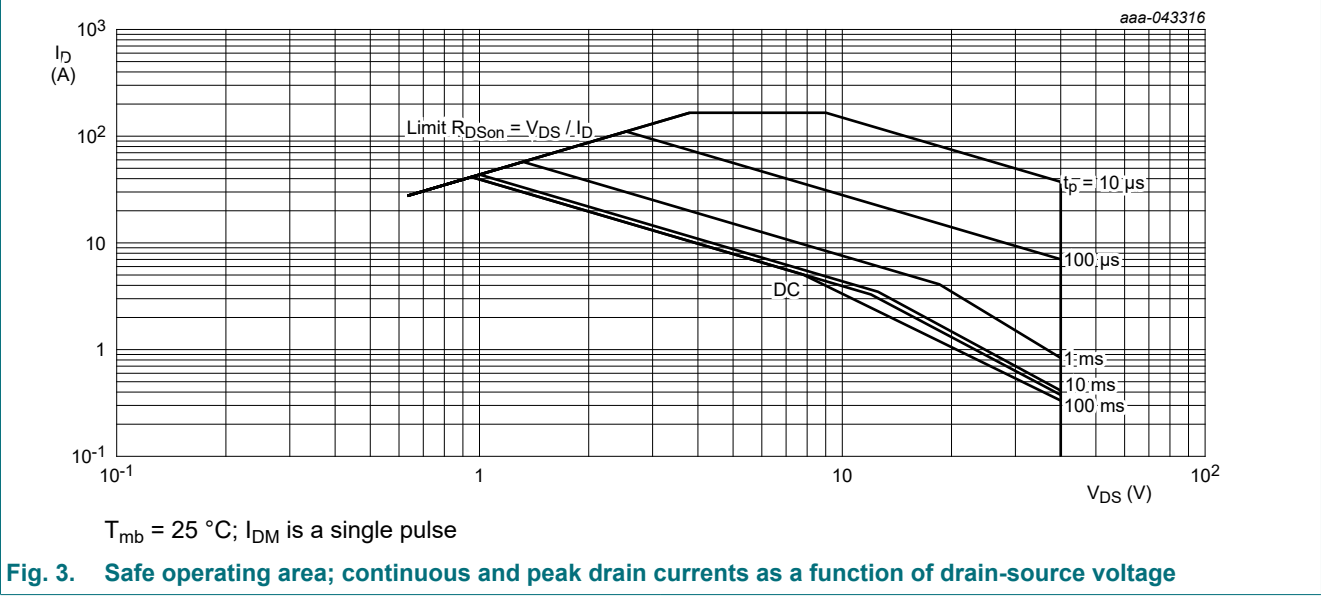
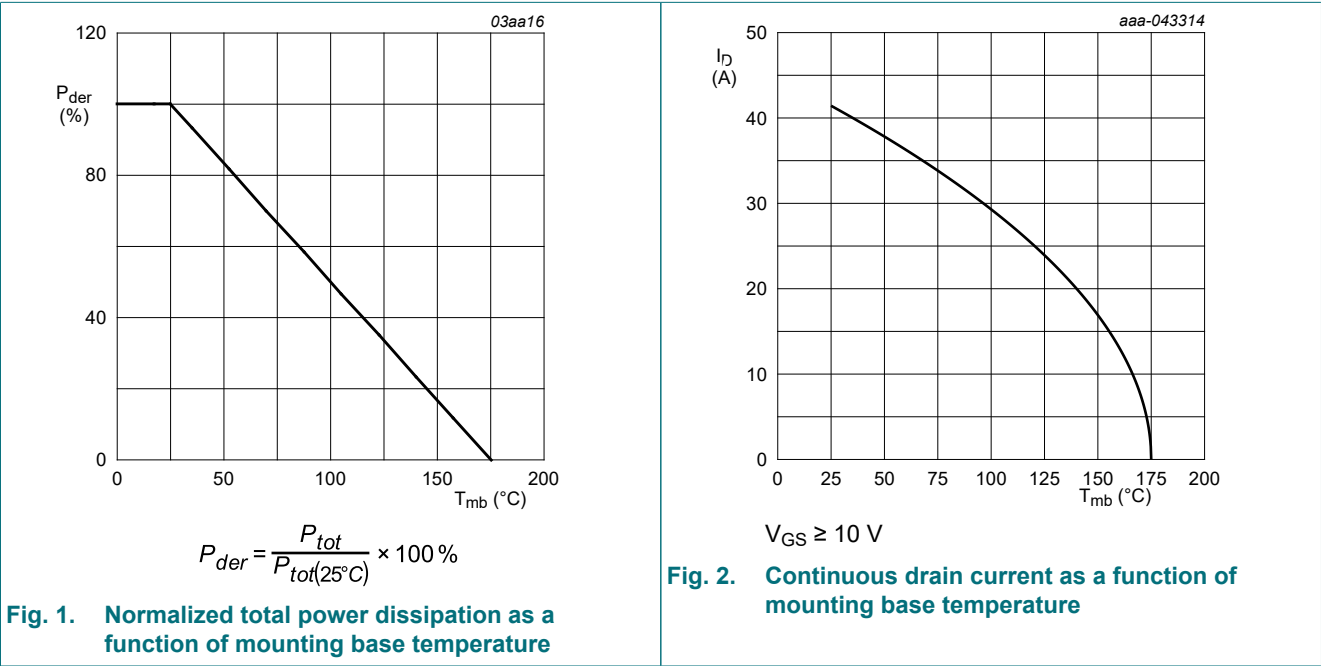
Table 5. Limiting values

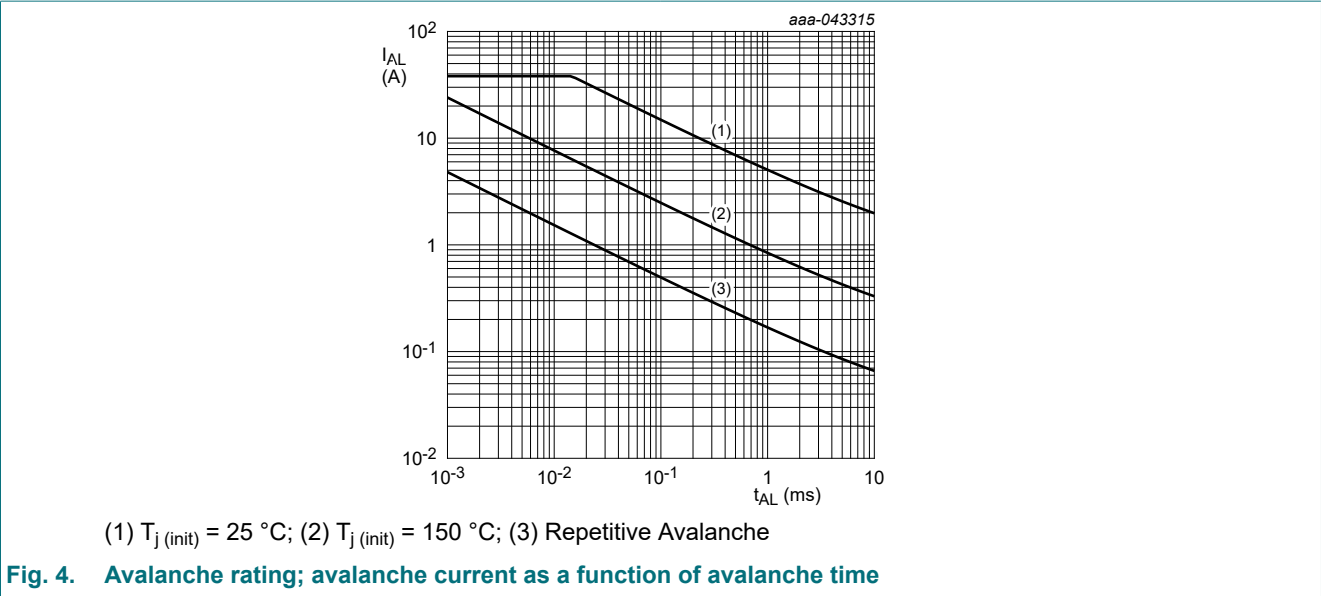
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	39	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	41	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	29	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	166	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	33	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	166	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 18.13\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped; $t_p = 66\ \mu\text{s}$; Fig. 4	[1] [2]	-	31.3	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $R_{GS} = 50\ \Omega$; Fig. 4	[3]	-	35	A

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.
- [3] Protected by 100% test



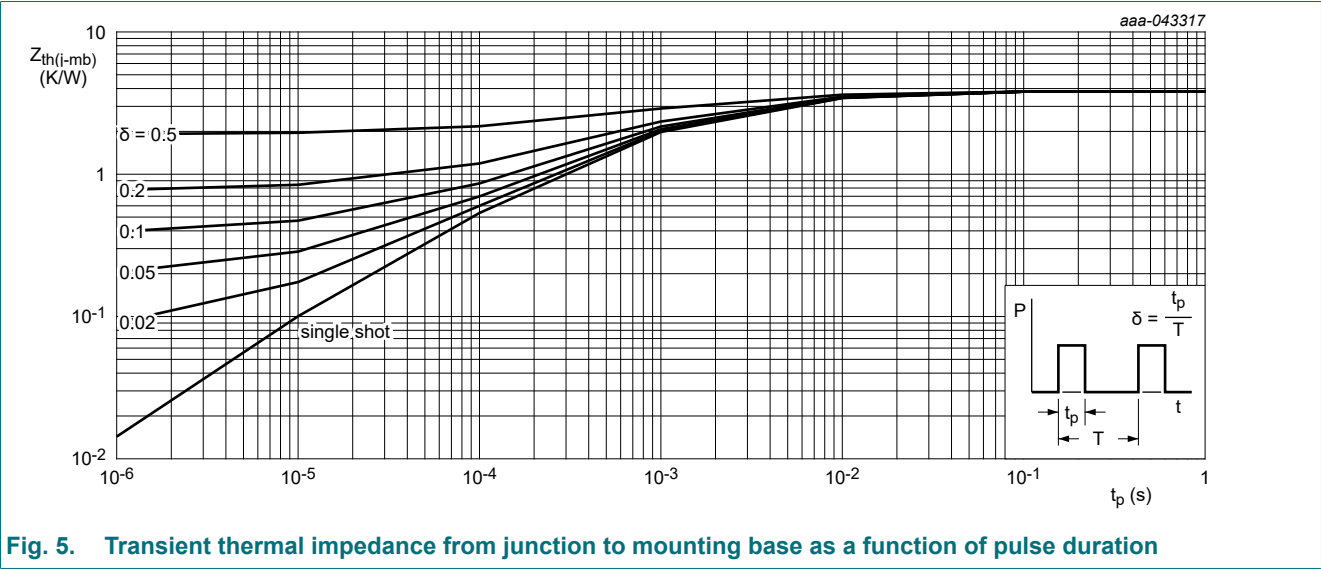


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	3.18	3.81	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	40	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	40	44	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_J = -40\ ^\circ\text{C}$	-	40.5	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_J = -55\ ^\circ\text{C}$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS}=V_{GS}$; $T_J = 25\ ^\circ\text{C}$; Fig. 9 ; Fig. 10	1.35	1.7	2.05	V
		$I_D = 1\ \text{mA}$; $V_{DS}=V_{GS}$; $T_J = 175\ ^\circ\text{C}$; Fig. 10	0.7	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS}=V_{GS}$; $T_J = -55\ ^\circ\text{C}$; Fig. 10	-	-	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 40\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	-	0.01	1	μA
		$V_{DS} = 40\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_J = 175\ ^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_J = 25\ ^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 25\ ^\circ\text{C}$; Fig. 11	7	10	12	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 105\ ^\circ\text{C}$; Fig. 12	9.4	14	17.8	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 125\ ^\circ\text{C}$; Fig. 12	10.1	15	19.3	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 175\ ^\circ\text{C}$; Fig. 12	12	18	23	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 25\ ^\circ\text{C}$; Fig. 11	9.1	13	15.6	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 105\ ^\circ\text{C}$; Fig. 12	12.2	17	23.1	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 125\ ^\circ\text{C}$; Fig. 12	13.2	18.6	25.1	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 10\ \text{A}$; $T_J = 175\ ^\circ\text{C}$; Fig. 12	15.6	22	29.8	m Ω
R_G	gate resistance	$f = 1\ \text{MHz}$; $T_J = 25\ ^\circ\text{C}$	0.85	2.1	5.4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ \text{A}$; $V_{DS} = 20\ \text{V}$; $V_{GS} = 10\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	-	13	18	nC
		$I_D = 10\ \text{A}$; $V_{DS} = 20\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	-	6	8.4	nC
Q_{GS}	gate-source charge	$I_D = 10\ \text{A}$; $V_{DS} = 20\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; $T_J = 25\ ^\circ\text{C}$; Fig. 13 ; Fig. 14	-	2.3	3.5	nC
Q_{GD}	gate-drain charge		-	1.4	2.8	nC
C_{iss}	input capacitance	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_J = 25\ ^\circ\text{C}$; Fig. 15	-	835	1169	pF
C_{oss}	output capacitance	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_J = 25\ ^\circ\text{C}$; Fig. 15	-	215	301	pF
C_{rss}	reverse transfer capacitance		-	37	81	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\ \text{V}$; $R_L = 2\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_{G(ext)} = 5\ \Omega$; $T_J = 25\ ^\circ\text{C}$	-	7	-	ns
t_r	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	11	-	ns
t_f	fall time		-	5	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 16		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	15	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17	[1]	-	7	-	nC

[1] includes capacitive recovery

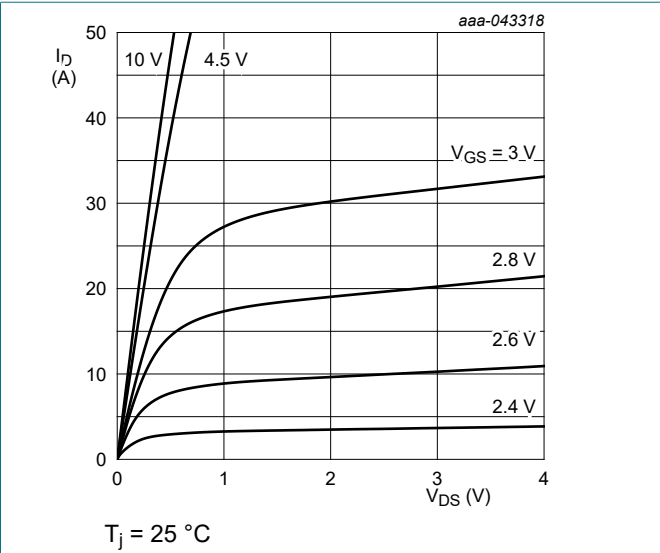


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

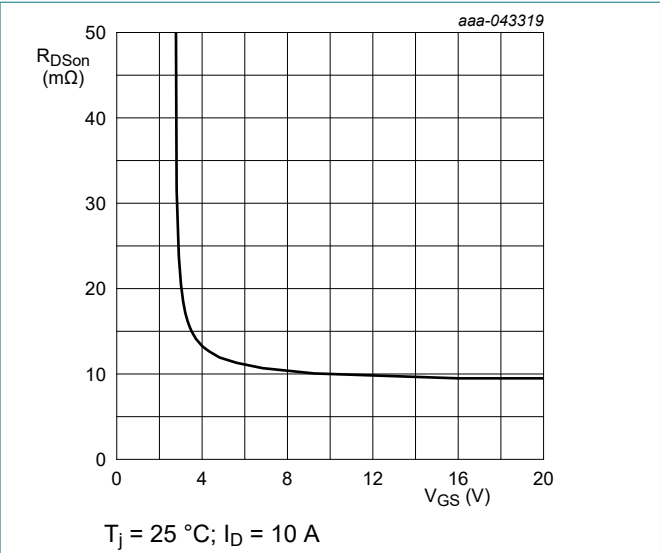


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

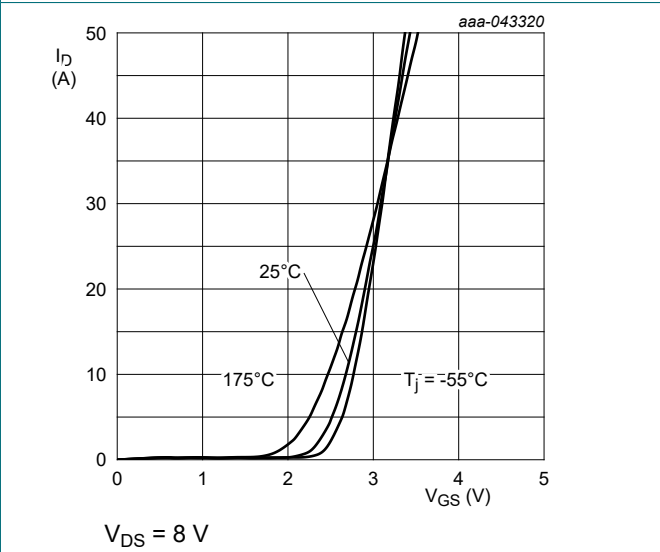


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

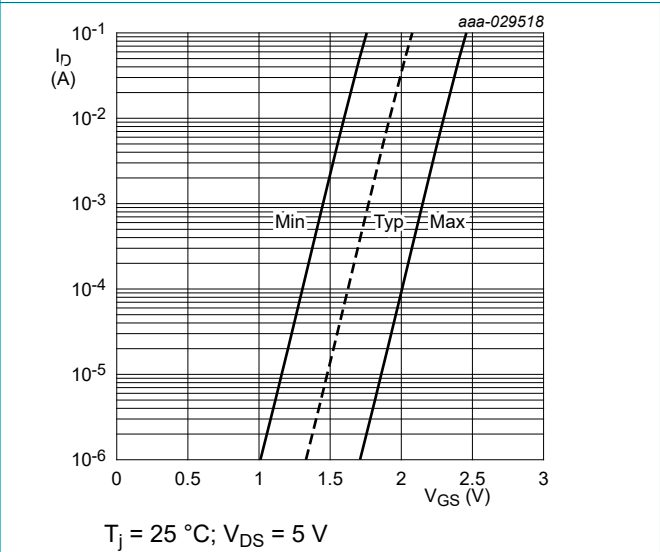


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

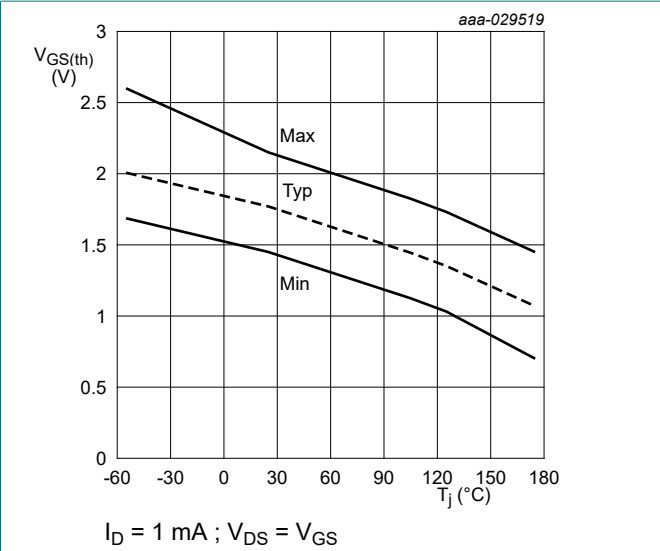


Fig. 10. Gate-source threshold voltage as a function of junction temperature

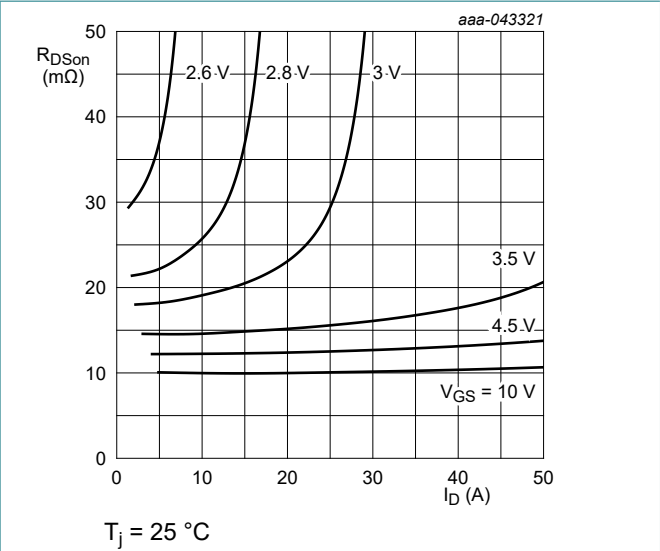


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

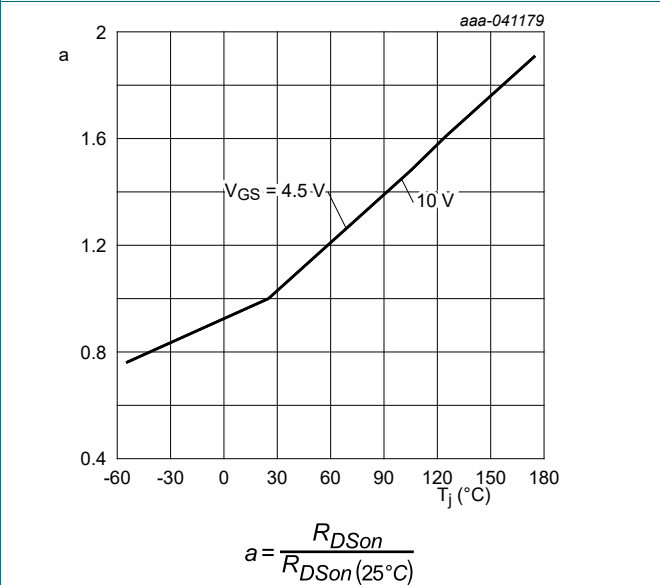


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

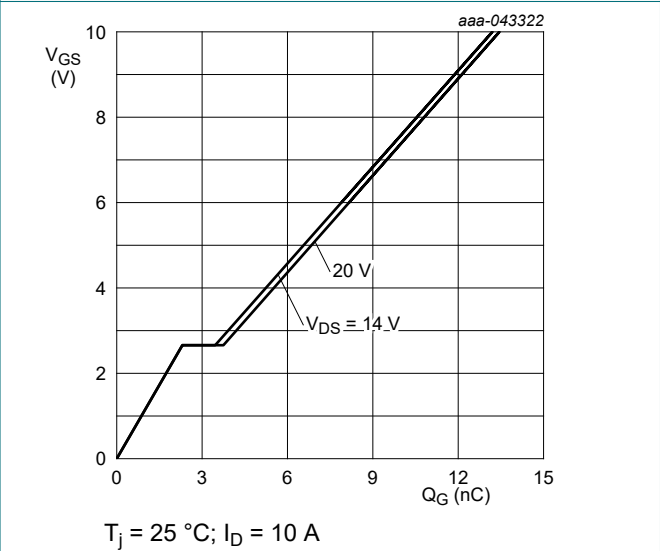


Fig. 13. Gate-source voltage as a function of gate charge; typical values

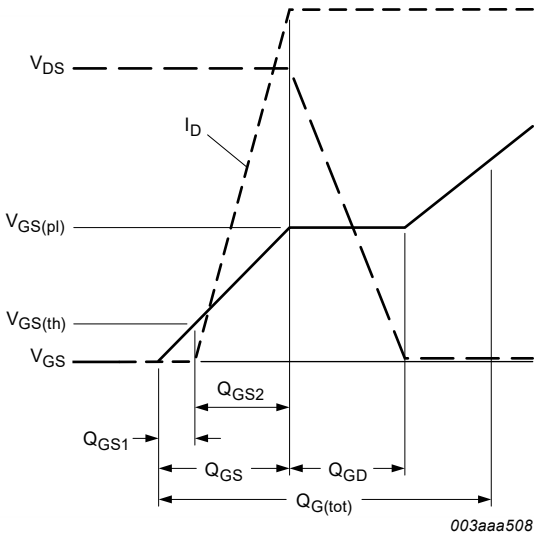


Fig. 14. Gate charge waveform definitions

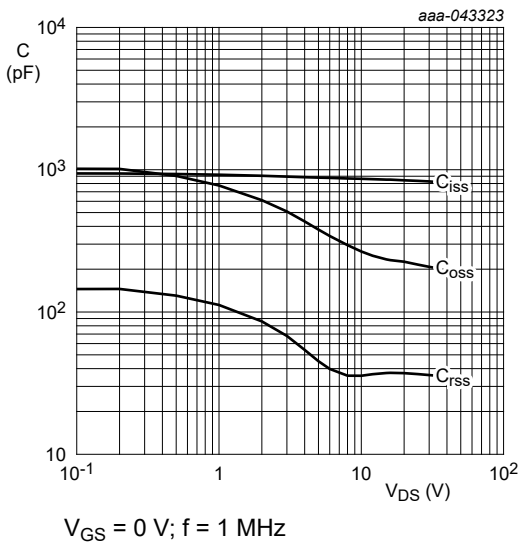


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

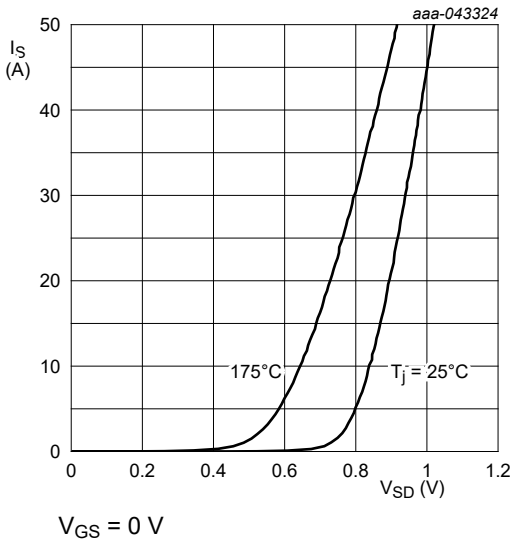


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

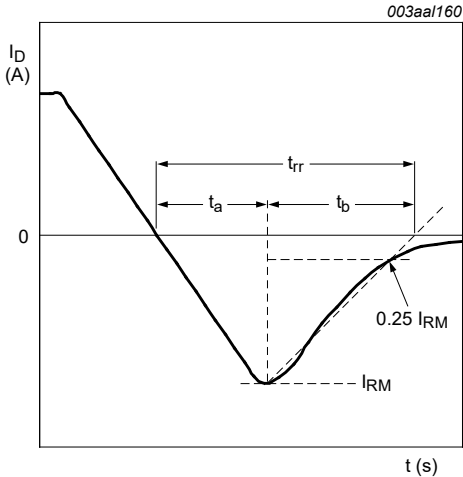


Fig. 17. Reverse recovery timing definition

11. Package outline

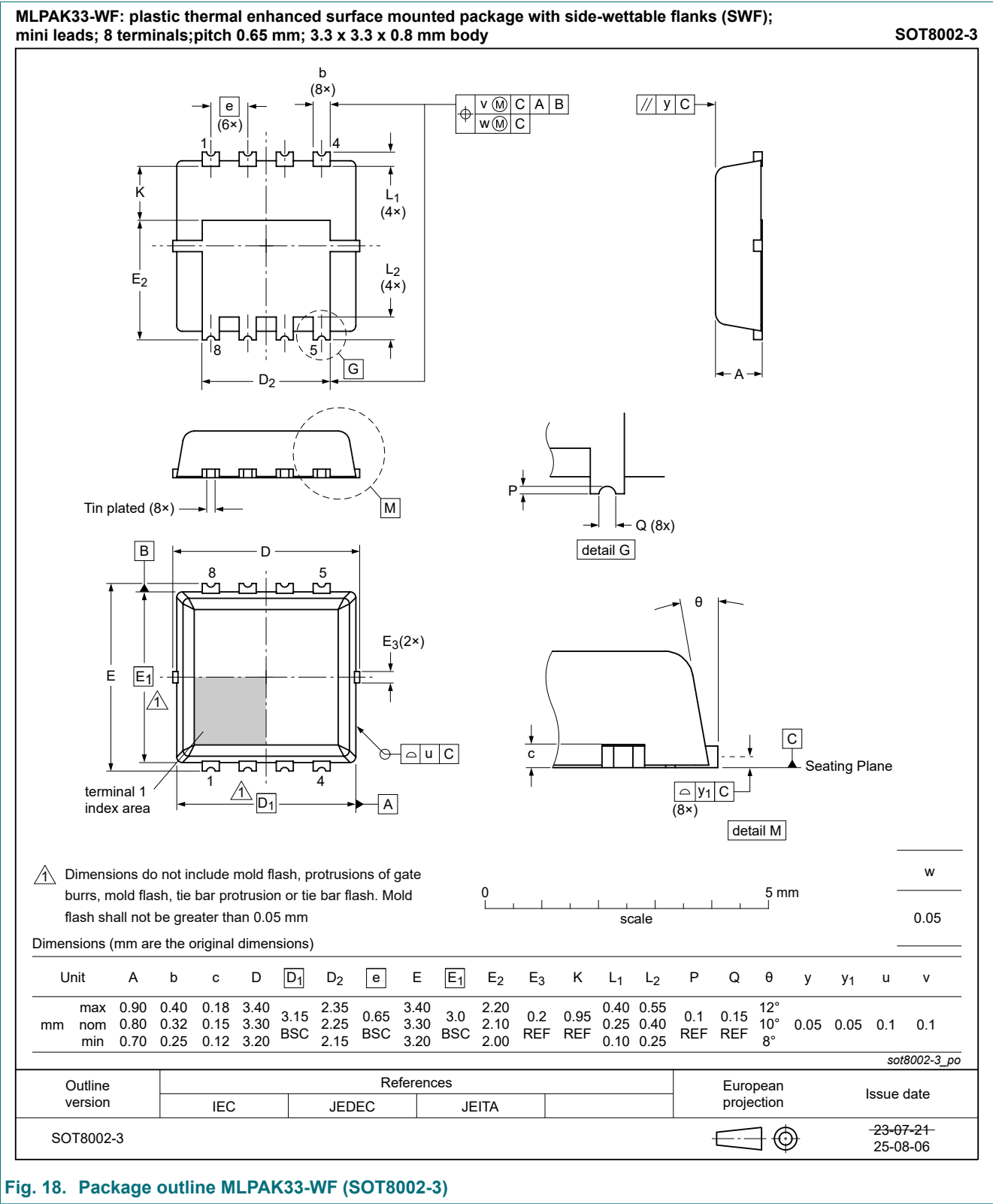


Fig. 18. Package outline MLPAK33-WF (SOT8002-3)

12. Soldering

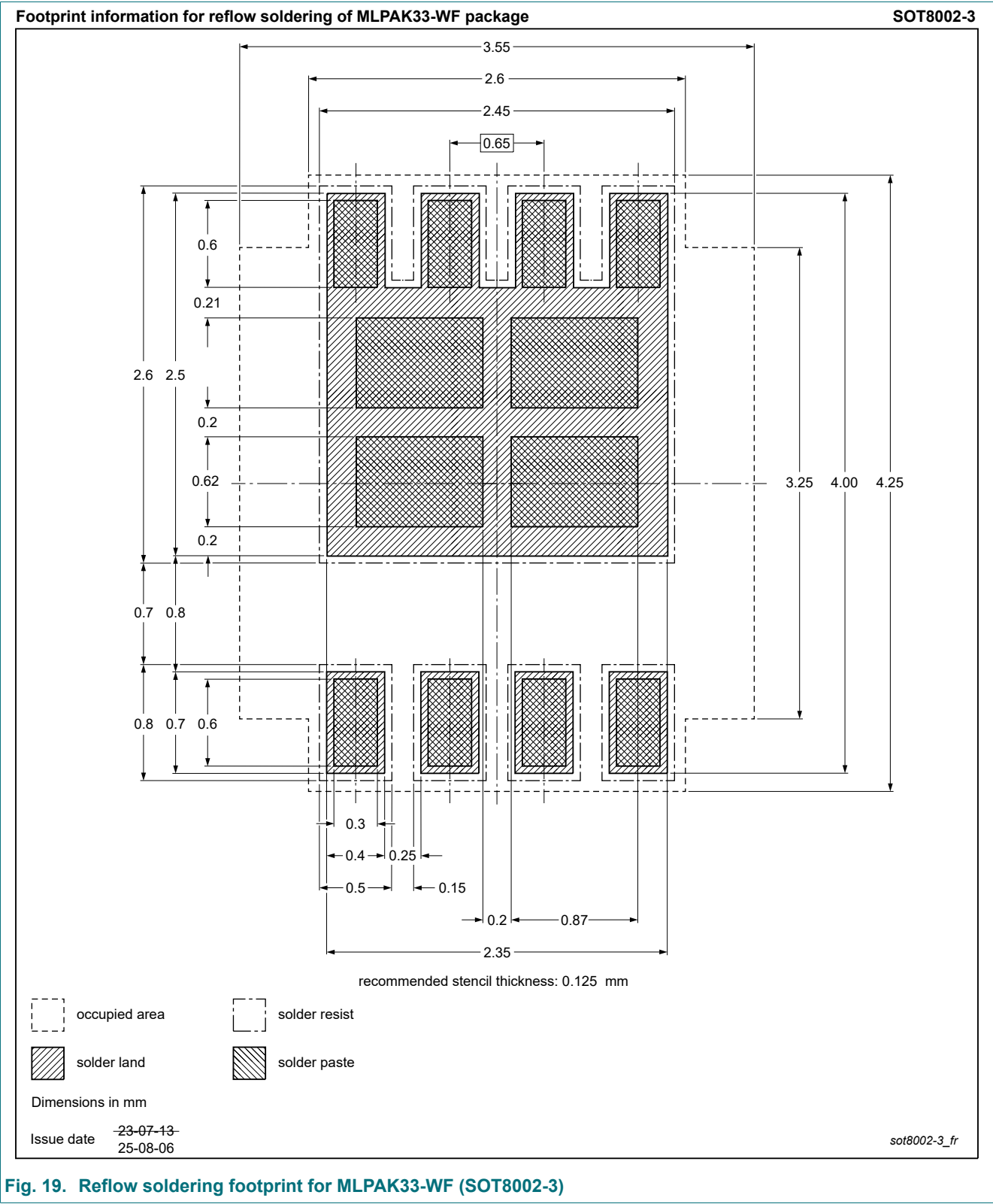


Fig. 19. Reflow soldering footprint for MLPAK33-WF (SOT8002-3)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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